

## Claims:

1. A video decoding circuit comprising:
  - a first video data processor;
  - 5 a second video data processor; and
  - a connection connecting said first video data processor and said second data processor;

wherein said first video data processor is arranged to receive a first signal comprising encoded video data, process

10 said first signal to provide a second signal and output said second signal, said first video data processor being arranged to process said first signal dependent on at least part of said received first signal, and

said second video data processor is arranged to receive

15 at least a part of said second signal, process said at least a part of said second signal to provide a third signal, and output said third signal, said second and third signals comprising a decoded video image stream, and

said second video data processor is arranged to process

20 said at least part of said second signal dependent on at least part of said at least part of second signal.
2. A circuit as claimed in claim 1, wherein said first video data processor is arranged to variable length decode
- 25 said received first signal to produce a decoded first signal.
3. A circuit as claimed in claim 2, wherein said first video data processor is arranged to separate said first signal data into at least a first part and a second part,
- 30 wherein said first part comprises at least one of:
  - pixel data;
  - residual data, and
  - wherein said second part comprises motion vector data.

4. A circuit as claimed in claim 3, wherein said first video data processor is arranged to inverse quantize said first part of said first signal.

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5. A circuit as claimed in claim 3 or 4, wherein said first video data processor is arranged to spatial domain transform said first part of said first signal.

10 6. A circuit as claimed in claims 4 or 5, wherein said first video data processor is arranged to combine said spatial domain transformed and/or inverse quantized first part of said first signal with said second part of said first signal.

15 7. A circuit as claimed in any previous claim, wherein said second video data processor is arranged to interpolate at least a first part of said second signal.

20 8. A circuit as claimed in claim 7, wherein said second video data processor is arranged to interpolate at least a first part of said second signal using one of horizontal and vertical interpolation.

25 9. A circuit as claimed in claim 8, further comprising a memory, said second video data processor being arranged to store said interpolated part of said second signal in said memory.

30 10. A circuit as claimed in claim 8 or 9, wherein said second video data processor is arranged to interpolate said stored interpolated first part of said second signal using the other one of horizontal and vertical interpolation.

11. A circuit as claimed in claims 7 to 10, wherein said second video data processor is arranged to combine said interpolated part of said second signal and a further part of said second signal,

5        wherein said interpolated part of said second signal comprises an estimated macro block, and said further part of said second signal comprises residual error data.

12. A circuit as claimed in any previous claim wherein said  
10 second video data processor is arranged to filter at least one of said at least one part of said second signal and said third signal.

13. A circuit as claimed in claim 12 wherein said filter  
15 comprises at least one of a de-ringing filter and a de-blocking filter.

14. A circuit as claimed in any previous claim, wherein said connection comprises a bus connecting said first and second  
20 video data processors.

15. A circuit as claimed in claim 14, further comprising a memory device, said memory device being connected to said bus.

25 16. A circuit as claimed in claim 15, wherein said first video data processor has an output for outputting said second signal to said memory device via said bus.

17. A circuit as claimed in claim 16, wherein said second  
30 video data processor has an input for receiving said parts of said second signal from said memory device via said bus.

18. A circuit as claimed in claims 1 to 17, wherein said connection comprises a data interconnect, said data

interconnect directly connecting said first video data processor and said second video data processor.

19. A circuit as claimed in claim 18, wherein said first  
5 video data processor has an output for outputting said second signal to said data interconnect.

20. A circuit as claimed in claim 18 and 19, wherein said  
10 second video data processor has an input for receiving said parts of said second signal from said data interconnect.

21. A circuit as claimed in claim 20 when appended to claim  
15 15, wherein said second video data processor receives part of said parts of said second signal from said data interconnect and part of said parts of said second signal from said bus.

22. A circuit as claimed in any previous claim, wherein said first signal is at least one of:

- 20 a MPEG2 encoded video stream;
- a H.263 encoded video stream;
- a RealVideo9 encoded video stream;
- a Windows media player encoded video stream;
- a H.264 encoded video stream.

25 23. A circuit as claimed in any previous claim, wherein said second signal comprises at least one of:

- buffer base address word;
- picture level parameter header word;
- picture level parameter word;
- 30 macro-block header word;
- slice parameter word;
- motion vector horizontal luma word;
- motion vector vertical luma word;
- motion vector horizontal chroma word;

motion vector vertical chroma word;  
pixel data reference word and  
pixel data residual word.

5 24. A circuit as claimed in any previous claim, wherein said first video data processor comprises a data packer.

25. A circuit as claimed in claims 1 to 23, wherein said second video data processor comprises a data packer.

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26. A circuit as claimed in claims 24 or 25, wherein said data packer comprises:

an input, said input being arranged to receive said second signal, said second signal comprising data words;

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means for ordering said data words; and

an output, said output being arranged to transmit data packets comprising ordered data words.

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27. An integrated circuit comprising a circuit as claimed in any previous claim.

28. A circuit as claimed in claims 1 to 26, wherein said first video data processor comprises a very long instruction word processor.

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29. A circuit as claimed in claim 28, wherein said very long instruction word processor is adapted to process said first signal further dependent on a set of instructions stored in a memory.

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30. A circuit as claimed in claims 1 to 29, wherein said second video data processor comprises a programmable processor.

31. A video decoding method comprising the steps of:

receiving at a first video data processor a first signal comprising encoded video data,

5 processing said first signal to provide a second signal dependent on at least part of said first signal,

outputting said second signal,

receiving at least a part of said second signal at a second video data processor,

10 processing said at least part of said second signal to provide a third signal dependent on at least part of said second signal, and

outputting said third signal,

wherein said second and third signals comprise a decoded video image stream.

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32. A method as claimed in claim 31, wherein said step of processing said first signal comprises the step of variable length decoding said first signal.

20 33. A method as claimed in claims 31 and 32, wherein said step of processing said first signal comprises the step of separating said first signal into at least a first part and a second part,

wherein said first part comprises at least one of:

25 pixel data;

residual data, and

wherein said second part comprises motion vector data.

30 34. A method as claimed in claim 33, wherein said step of processing said first signal further comprises the step of inverse quantizing said first part of said first signal.

35. A method as claimed in claims 33 and 34, wherein said step of processing said first signal further comprises the

step of spatial domain transforming said first part of said first signal.

36. A method as claimed in claims 34 or 35, wherein said step  
5 of processing said first signal further comprises the step of combining said spatial domain transformed and/or inverse quantized first part of said first signal with said second part of said first signal.

10 37. A method as claimed in claims 31 to 36, wherein said step of processing at least a part of said second signal further comprises the step of interpolating at least a first part of said second signal.

15 38. A method as claimed in claim 37, wherein said step of interpolating at least a first part of said second signal comprises the step of interpolating at least a first part of said second signal using one of horizontal and vertical interpolation.

20 39. A method as claimed in claim 38, wherein said step of interpolating further comprises storing said interpolated part of said second signal.

25 40. A method as claimed in claims 38 and 39, wherein said step of interpolating further comprises interpolating said interpolated part of said second signal using the other one of horizontal and vertical interpolation.

30 41. A method as claimed in claims 37 to 40, wherein said step of processing at least part of said second signal further comprises combining said interpolated part of said second signal and a further part of said second signal, wherein said interpolated part of said second signal comprises an estimated

macro block, and said further part of said second signal comprises residual error data.

42. A method as claimed in claims 31 to 41, wherein said step  
5 of processing at least a part of said second signal further comprises the step of filtering, wherein said step of filtering comprises at least one of the steps:

de-ringing filtering and de-blocking filtering.

10 43. A method as claimed in claims 31 to 42, wherein said step of outputting said second signal further comprises the step of storing said second signal in a memory.

44. A method as claimed in claims 31 to 43, wherein said step  
15 of receiving at least part of said second signal comprises receiving said at least part of said second signal directly from the first video data processor.

45. A method as claimed in claims 44 when appended to claim  
20 40, wherein said step of receiving at least part of said second signal comprises receiving a first part of said at least part of said second signal directly from said first video data processor and a second part of said at least part of said second signal from said memory.

25 46. A method as claimed in claim 31 to 45, wherein said step of processing said first signal further comprises the step of packetizing said second signal.

30 47. A method as claimed in claims 31 to 45, wherein said step of processing said second signal further comprises the steps of:

packetizing said at least part of said second signal;

storing said at least part of said second signal in a memory; and

receiving said at least part of said stored second signal from said memory.

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48. A video decoding circuit comprising:

a first video data processor (509);

a second video data processor (519); and

a connection connecting said first video data processor

10 and said second data processor;

wherein said first video data processor (509) is arranged to receive a first signal comprising encoded video data, process said first signal to provide a second signal and output said second signal, said first video data processor  
15 (509) being arranged to process said first signal dependent on at least part of said received first signal, and

said second video data processor (519) comprising a predictor constructor 419, said second video data processor (519) is arranged to receive at least a part of said second  
20 signal, process said at least a part of said second signal to provide a third signal, and output said third signal, said second and third signals comprising a decoded video image stream, and characterised wherein a part of said second signal comprises a picture level parameter word which comprises  
25 coding standard information, said coding standard information defining variations in the type of data and  
said second video data processor (519) predictor constructor (459) is arranged to process said at least part of said second signal dependent on the format of the data received

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49. A video decoding method comprising the steps of:

receiving at a first video data processor (509) a first signal comprising encoded video data,

processing said first signal to provide a second signal  
dependent on at least part of said first signal,  
outputting said second signal,  
receiving at least a part of said second signal at a  
5 second video data processor (519),  
processing said at least part of said second signal  
within the second video processor (519) predictor constructor  
(459) to provide a third signal, and  
outputting said third signal,  
10 wherein said second and third signals comprise a decoded video  
image stream, characterised wherein said step of outputting  
said second signal comprises the step of outputting coding  
standard information, the coding standard information defining  
variations in the type of data, and said step of processing  
15 said at least part of said second signal is dependent on the  
format of the video data received.

## AMENDED CLAIMS

[(received by the International Bureau on 03 May 2005 (03.05.05);  
original claims 1-49 replaced by amended claims 1-47 (9 pages)]

1. A video decoding circuit comprising:
  - a first video data processor (509);
  - 5 a second video data processor (519); and
  - a connection connecting said first video data processor and said second data processor;

wherein said first video data processor (509) is arranged to receive a first signal comprising encoded video data, process said first signal to provide a second signal and output said second signal, said first video data processor (509) being arranged to process said first signal dependent on at least part of said received first signal, and

said second video data processor (519) comprising a predictor constructor 419, said second video data processor (519) is arranged to receive at least a part of said second signal, process said at least a part of said second signal to provide a third signal, and output said third signal, said second and third signals comprising a decoded video image stream, wherein a part of said second signal comprises a picture level parameter word which comprises coding standard information, said coding standard information defining variations in the type of data and

said second video data processor (519) predictor constructor (459) is arranged to process said at least part of said second signal dependent on the format of the data received.
2. A circuit as claimed in claim 1, wherein said first video data processor (509) is arranged to variable length decode said received first signal to produce a decoded first signal.

3. A circuit as claimed in claim 2, wherein said first video data processor (509) is arranged to separate said first signal data into at least a first part and a second part, wherein said first part comprises at least one of:
- 5 pixel data;  
residual data, and  
wherein said second part comprises motion vector data.
4. A circuit as claimed in claim 3, wherein said first video data processor (509) is arranged to inverse quantize said first part of said first signal.
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5. A circuit as claimed in claim 3 or 4, wherein said first video data processor (509) is arranged to spatial domain transform said first part of said first signal.
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6. A circuit as claimed in claims 4 or 5, wherein said first video data processor (509) is arranged to combine said spatial domain transformed and/or inverse quantized first part of said first signal with said second part of said first signal.
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7. A circuit as claimed in any previous claim, wherein said second video data processor (519) is arranged to interpolate at least a first part of said second signal.
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8. A circuit as claimed in claim 7, wherein said second video data processor (519) is arranged to interpolate at least a first part of said second signal using one of horizontal and vertical interpolation.
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9. A circuit as claimed in claim 8, further comprising a memory (501), said second video data processor being arranged to store said interpolated part of said second signal in said memory (501).

10. A circuit as claimed in claim 8 or 9, wherein said second video data processor (519) is arranged to interpolate said stored interpolated first part of said second signal using the  
5 other one of horizontal and vertical interpolation.

11. A circuit as claimed in claims 7 to 10, wherein said second video data processor (519) is arranged to combine said interpolated part of said second signal and a further part of  
10 said second signal,

wherein said interpolated part of said second signal comprises an estimated macro block, and said further part of said second signal comprises residual error data.

12. A circuit as claimed in any previous claim wherein said second video data processor (519) is arranged to filter at least one of said at least one part of said second signal and said third signal.  
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13. A circuit as claimed in claim 12 wherein said filter comprises at least one of a de-ringing filter and a de-blocking filter.  
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14. A circuit as claimed in any previous claim, wherein said connection comprises a bus (503) connecting said first and second video data processors.  
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15. A circuit as claimed in claim 14, further comprising a memory device (501), said memory device being connected to said bus (503).  
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16. A circuit as claimed in claim 15, wherein said first video data processor (509) has an output for outputting said second signal to said memory device (501) via said bus (503).

17. A circuit as claimed in claim 16, wherein said second video data processor (519) has an input for receiving said parts of said second signal from said memory device (501) via  
5 said bus.

18. A circuit as claimed in claims 1 to 17, wherein said connection comprises a data interconnect (511), said data interconnect (511) directly connecting said first video data  
10 processor (509) and said second video data processor (519).

19. A circuit as claimed in claim 18, wherein said first video data processor (509) has an output for outputting said second signal to said data interconnect (511).  
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20. A circuit as claimed in claim 18 and 19, wherein said second video data processor (519) has an input for receiving said parts of said second signal from said data interconnect (511).  
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21. A circuit as claimed in claim 20 when appended to claim 15, wherein said second video data processor (519) receives part of said parts of said second signal from said data interconnect (511) and part of said parts of said second  
25 signal from said bus (503).

22. A circuit as claimed in any previous claim, wherein said first signal is at least one of:

- 30 a MPEG2 encoded video stream;
- a H.263 encoded video stream;
- a RealVideo9 encoded video stream;
- a Windows media player encoded video stream;
- a H.264 encoded video stream.

23. A circuit as claimed in any previous claim, wherein said second signal further comprises at least one of:

- buffer base address word;
- picture level parameter header word;
- 5 macro-block header word;
- slice parameter word;
- motion vector horizontal luma word;
- motion vector vertical luma word;
- motion vector horizontal chroma word;
- 10 motion vector vertical chroma word;
- pixel data reference word and
- pixel data residual word.

24. A circuit as claimed in any previous claim, wherein said  
15 first video data processor (509) comprises a data packer.

25. A circuit as claimed in claims 1 to 23, wherein said second video data processor (519) comprises a data packer (419).

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26. A circuit as claimed in claims 24 or 25, wherein said data packer (419) comprises:

- an input (851), said input being arranged to receive said second signal, said second signal comprising data words;
- 25 means for ordering said data words (801); and
- an output (855), said output being arranged to transmit data packets comprising ordered data words.

27. An integrated circuit comprising a circuit as claimed in  
30 any previous claim.

28. A circuit as claimed in claims 1 to 26, wherein said first video data processor (509) comprises a very long instruction word processor.

29. A circuit as claimed in claim 28, wherein said very long instruction word processor is adapted to process said first signal further dependent on a set of instructions stored in a memory.

30. A circuit as claimed in claims 1 to 29, wherein said second video data processor (519) comprises a programmable processor.

31. A video decoding method comprising the steps of:  
receiving at a first video data processor (509) a first signal comprising encoded video data,  
processing said first signal to provide a second signal dependent on at least part of said first signal,  
outputting said second signal,  
receiving at least a part of said second signal at a second video data processor (519),  
processing said at least part of said second signal within the second video processor (519) predictor constructor (459) to provide a third signal, and  
outputting said third signal,  
wherein said second and third signals comprise a decoded video image stream, wherein said step of outputting said second signal comprises the step of outputting coding standard information, the coding standard information defining variations in the type of data, and said step of processing said at least part of said second signal is dependent on the format of the video data received.

32. A method as claimed in claim 31, wherein said step of processing said first signal comprises the step of variable length decoding said first signal.

33. A method as claimed in claims 31 and 32, wherein said step of processing said first signal comprises the step of separating said first signal into at least a first part and a second part,

- 5        wherein said first part comprises at least one of:  
         pixel data;  
         residual data, and  
         wherein said second part comprises motion vector data.

- 10    34. A method as claimed in claim 33, wherein said step of processing said first signal further comprises the step of inverse quantizing said first part of said first signal.

- 15    35. A method as claimed in claims 33 and 34, wherein said step of processing said first signal further comprises the step of spatial domain transforming said first part of said first signal.

- 20    36. A method as claimed in claims 34 or 35, wherein said step of processing said first signal further comprises the step of combining said spatial domain transformed and/or inverse quantized first part of said first signal with said second part of said first signal.

- 25    37. A method as claimed in claims 31 to 36, wherein said step of processing at least a part of said second signal further comprises the step of interpolating at least a first part of said second signal.

- 30    38. A method as claimed in claim 37, wherein said step of interpolating at least a first part of said second signal comprises the step of interpolating at least a first part of said second signal using one of horizontal and vertical interpolation.

39. A method as claimed in claim 38, wherein said step of interpolating further comprises storing said interpolated part of said second signal.

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40. A method as claimed in claims 38 and 39, wherein said step of interpolating further comprises interpolating said interpolated part of said second signal using the other one of horizontal and vertical interpolation.

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41. A method as claimed in claims 37 to 40, wherein said step of processing at least part of said second signal further comprises combining said interpolated part of said second signal and a further part of said second signal, wherein said  
15 interpolated part of said second signal comprises an estimated macro block, and said further part of said second signal comprises residual error data.

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42. A method as claimed in claims 31 to 41, further comprising a further step of further processing at least a part of said second signal, wherein said further processing step comprises the step of filtering, wherein said step of filtering comprises at least one of the steps:

de-ringing filtering and de-blocking filtering.

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43. A method as claimed in claims 31 to 42, wherein said step of outputting said second signal further comprises the step of storing said second signal in a memory (501).

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44. A method as claimed in claims 31 to 43, wherein said step of receiving at least part of said second signal comprises receiving said at least part of said second signal directly from the first video data processor (509).

45. A method as claimed in claims 44 when appended to claim 40, wherein said step of receiving at least part of said second signal comprises receiving a first part of said at least part of said second signal directly from said first video data processor (509) and a second part of said at least part of said second signal from said memory (501).

46. A method as claimed in claim 31 to 45, wherein said step of processing said first signal further comprises the step of packetizing said second signal.

47. A method as claimed in claims 31 to 45, further comprising the steps of:

packetizing said at least part of said second signal;  
15 storing said at least part of said second signal in a memory; and

receiving said at least part of said stored second signal from said memory.